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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/236,526	01/25/1999	FELIX KHOURI	081862.P119	1370

7590 01/16/2002

BLAKELY SOKOLOFF TAYLOR AND ZAFMAN
SEVENTH FLOOR
12400 WILSHIRE BOULEVARD
LOS ANGELES, CA 90025

EXAMINER

SPAFFORD, TIMOTHY J

ART UNIT	PAPER NUMBER
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2662

DATE MAILED: 01/16/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/236,526

Applicant(s)

KHOURI ET AL.

Examiner

Tim Spafford

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☐ Responsive to communication(s) filed on ____.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-17 is/are pending in the application.
- 4a) Of the above claim(s) ____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) ____ is/are allowed.
- 6) ☒ Claim(s) 1-17 is/are rejected.
- 7) ☐ Claim(s) ____ is/are objected to.
- 8) ☐ Claim(s) ____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on ____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on ____ is: a) ☐ approved b) ☐ disapproved by the Examiner.
If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. ____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
* See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892) 4) ☐ Interview Summary (PTO-413) Paper No(s). ____
- 2) ☒ Notice of Draftsperson's Patent Drawing Review (PTO-948) 5) ☐ Notice of Informal Patent Application (PTO-152)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) ____ 6) ☐ Other: ____

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claims 1-17 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 1, 7, 9, 10 and 16 recite, in the second to last line of each claim, the phrase "first set of errors" but there is no definition in the claims or specification as to how this set is determined, thereby rendering these claims indefinite. Additionally, each claim recites the phrase "determining if a threshold has been reached" but does not define what is being compared to the threshold.

Claims 2-8 and 11-17 depend from a rejected claim and include all of the limitations of that rejected claim thereby rendering these dependent claims indefinite.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. Claims 1-2, 5-7, 9-11 and 14-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ozaki (USPN 6,124,802) in view of Key et al. (USPN 6,173,386).

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Referring to claims 1, 9 and 10, Ozaki shows, in column 6 line 47 thru column 7 line 10, a method/apparatus for managing a selectively called radio receiver having a processor card including memory and a processing unit in the processor card comprising the following steps/means or an article comprising a computer readable medium having instructions stored thereon, which when executed, causes the following:

detecting an error;

determining whether a threshold has been reached; and

performing a re-initialization/rebuild in the processor card when the threshold is reached.

Ozaki fails to show that the method/apparatus is used to manage a network switch; the step/means of determining the type of error; and performing a hitless rebuild when the type of error is in a first set of errors and the threshold has not been reached. Key et al. show, in column 1 lines 38-58, that the same architecture is used to manage a network switch. Keys et al. further show, in column 18 lines 22-63, the processing unit determining the type of error. Neither reference explicitly states that the rebuild should occur if the error is in a first set of errors and the threshold has not been reached. However, as is known in the art, the software in the processing unit could be modified to perform in this manner since the threshold and type of error are known.

It would have been obvious to one skilled in the art at the time of the invention to use the network switch architecture and error determination method as taught by Key et al. with the method/apparatus of Ozaki to reduce the amount of service disruptions for devices connected to the switch nodes.

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Referring to claims 2 and 11, Ozaki shows, in figure 3 and column 6 lines 47-60, the method/article wherein the step of performing the hitless rebuild includes performing an initialization of the memory and protecting a portion of the memory from access by the processing unit during initialization. The ROM region of memory would not be affected by performing a memory initialization.

Referring to claims 5 and 14, Ozaki shows, in figure 3 and column 6 lines 47-60, the method/article wherein the memory is accessed through a set of memory addresses and performing a hitless rebuild includes preventing the processing unit from accessing a predetermined set of memory addresses in the set of memory addresses (write prohibit region).

Referring to 6 and 15, Ozaki shows everything discussed for claims 1 and 10 above. Ozaki fails to show the method/article wherein determining the type of error includes identifying a non-ignorable error. Key et al. show, in column 18 lines 22-45, a detector determining whether the error is of a type that is considered fatal/non-recoverable/non-ignorable. It would have been obvious to one skilled in the art at the time of the invention to combine the identification of non-ignorable errors as taught by Key et al. with the method/article of Ozaki to save processing time by processing each error type differently.

Referring to claims 7 and 16, Ozaki shows everything discussed for claims 1 and 10 above. Ozaki fails to show the method/article further including setting the processing unit to enter into a degraded mode when the type of the error is in the first set of errors and the threshold has been reached. Key et al. show, in column 5 lines 21-38, a

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processor may be configured such that, depending on the type of event(s) encountered, it may be made to enter a debug or degraded mode. It would have been obvious to one skilled in the art at the time of the invention to combine the configuration capability as taught by Key et al. with the method/article of Ozaki to make it easier to determine specific sources of improper processor operation.

5. Claims 3-4 and 12-13 rejected under 35 U.S.C. 103(a) as being unpatentable over Ozaki (USPN 6,124,802) in view of Key et al. (USPN 6,173,386) as applied to claims 1 and 10 above, and further in view of the prior art as defined in the Academic Press Dictionary of Science & Technology.

Ozaki and Key et al. show everything discussed for claims 1 and 10 above. They fail to show the method/article wherein performing a hitless rebuild includes protecting a portion of the memory that contains a set of routing or state tables. The Academic Press Dictionary of Science & Technology defines memory or storage protection as the limitation of access to main memory so that only the program/application to which a memory area is assigned can access it. So the portion of memory that stores the routing or state tables can be protected from the hitless rebuild application. It would have been obvious to one skilled in the art at the time of the invention to use the memory protection as taught by the prior art with the method/article as taught by Ozaki and Key et al. to save processing time by not rebuilding these tables.

Allowable Subject Matter

6. Claims 8 and 17 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a. Simmons (USPN 6,185,630) discloses a device initializing system with programmable array logic.

b. Brey et al. (USPN 5,274,646) discloses an excessive error correction control method.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tim Spafford whose telephone number is (703) 306-4820. The examiner can normally be reached on 7:30 - 4:30 M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Hassan Kizou can be reached on (703) 305-4744. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 872-9314 for regular communications and (703) 872-9314 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to customer service whose telephone number is (703) 306-0377.

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tjs

January 10, 2002

A handwritten signature in black ink, appearing to read 'Hassan Kizou', is positioned above the printed name.

HASSAN KIZOU
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600